# Application Note

**Document No.: AN1132**

**G32R5xx Zidian Application Note**

**Version: V1.1**

# 1 Introduction

This application note introduces G32R5xx Zidian, including a basic overview and software design examples.

# Contents

# 2 Zidian Overview

Zidian is a mathematical extension instruction set designed for the G32R5xx series real-time control MCU. It can effectively improve the performance of mathematical operations.

## 2.1 ICAU and FCAU

On the software side, Zidian is exposed through “driverlib/<device>/driverlib/zidian_cde.h” and “zidian_math.h”. **The header contents for G32R501 and G32R502 are not identical**: floating-point acceleration (FCAU) is shared on both devices; integer-side (ICAU) capability is device-trimmed. Before selecting APIs, check Table 1 and open the headers under the matching device directory to confirm macro names.

**Note:** Table 1 reflects current SDK headers and indicates whether this SDK provides the given wrapper/macro. Silicon instruction details follow the datasheet.

Table 1 Zidian common interface support (by function family)

| No. | Function family | Representative symbols / header | G32R501 | G32R502 |
|---|---|---|---|---|
| 1 | FCAU sine / cosine | “sinpuf32” / “sin” / “cospuf32” / “cos”; under “ZIDIAN_FCAU”: “sinf” / “cosf” | Y | Y |
| 2 | FCAU arctangent | “atan*” / “atan2*” / “quadf32” / “divf32_atan2”; “atanf” / “atan2f” | Y | Y |
| 3 | FCAU sqrt / divide / 2π scale | “sqrtf32” / “divf32” / “mpy2pif32” / “div2pif32”; “sqrtf” | Y | Y |
| 4 | VCX assembly mnemonic macros | “SINPUF32” / “COSPUF32” / “ATANPUF32” / “SQRTF32”, etc. | Y | Y |
| 5 | VCX C short-name wrappers (502 naming) | “sinpu” / “cospu” / “atanpu” / “sqrt” / “div” / “quad”, etc. | — | Y |
| 6 | CRC (“zidian_cde.h” macros) | “crc8l/h”, “crc16p1l/h”, “crc16p2l/h”, “crc32l/h” | Y | Y |
| 7 | CRC (“zidian_math.h” inline wrappers) | “crc8l32” … “crc32h32” | — | Y |

| No. | Function family | Representative symbols / header | G32R501 | G32R502 |
|---|---|---|---|---|
| 8 | 64-bit division | “div64re” / “div64uu” / “div64iu” / “div64ii”; “div6464” | — | Y |
| 9 | CX2 status / negate | “tas” / “rstatus” / “wstatus” / “neg” | Y | — |
| 10 | CX3 shift-add/sub | “sh1add*” / “sh1sub*” (12 symbols) | Y | — |
| 11 | CX3D butterfly / max | “hstas” / “hstsa” / “lstas” / “lstsa” / “max” | Y | — |
| 12 | CX3DA bit select | “hbitsel” | Y | — |
| 13 | FFT / butterfly assembly macros | “VITBM2” / “VITBM3” / “VITDHADDSUB” / “VITDL” / “VITLSEL” / “VTRACE”, etc. | Y | — |
| 14 | Complex add/MAC assembly macros | “VCADD” / “VCSUB” / “VCMPY” / “VCMAC” / “VCDADD16” / “VCDSUB16”, etc. | Y | — |

## 2.2 G32R501 / G32R502 differences

- **FCAU (floating-point) is shared:** after defining “ZIDIAN_FCAU” and including “zidian_math.h”, “sinf” / “cosf” / “atanf” / “atan2f” / “sqrtf” can be redirected to Zidian-accelerated implementations.
- **G32R501 integer focus is SIMD / FFT / complex:** “zidian_cde.h” provides CX3/CX3D (for example “sh1add”, “hstas”, “max”) and assembly macros such as “VCMPY”, “VCADD”, and “VITBM” for FFT and complex workloads.
- **G32R502 current SDK does not provide FFT / complex macro wrappers:** the 502 “zidian_cde.h” has **no** “sh1add”, “hstas”, or “max”, and no “VCMPY” / “VCADD” / “VITBM” symbols. For SIMD FFT or complex math, **do not** call those 501-style macros; use ordinary software algorithms, or confirm whether another library is available.
- **G32R502 integer focus is CRC wrappers and 64-bit division:** both devices expose “crc*” macros in “zidian_cde.h”; **only 502** further wraps “crc*32” in “zidian_math.h” and provides “div64*” / “div64*64”.
- **Use device-specific paths:** G32R501 uses “driverlib/g32r501/driverlib/zidian_*.h”; G32R502 uses “driverlib/g32r502/driverlib/zidian_*.h”. Do not mix them.

In G32R5xx software, extensions are commonly grouped as CDE and FPCDE.

For CDE extensions, instructions operate on general-purpose registers to improve integer performance. This capability set is the integer computation acceleration unit (ICAU). **Exposure differs by device:**

- G32R501: CRC macros plus SIMD-oriented shift-add/sub, butterfly, and FFT/complex wrappers (see Table 1 rows 9–14).
- G32R502: CRC macros and 64-bit division wrappers; **without** the FFT / complex / CX3·CX3D application macros in Table 1.

For FPCDE extensions, instructions operate on floating-point registers to improve floating-point performance (trigonometric functions, square root, division, and related operations). This capability set is the floating-point computation acceleration unit (FCAU). **Both G32R501 and G32R502 support FCAU** (see Table 1 rows 1–5).

## 2.3 CDE built-in functions

By introducing standardized CDE built-in functions as part of the Arm C language extension, Tables 2 and 3 list the built-in functions supported by Zidian.

Table 2 Built-in functions supported by ICAU

| Instruction type | Built-in functions |
|---|---|
| CX2 | uint32_t __arm_cx2(int coproc, uint32_t n, uint32_t imm); |
| CX2A | uint32_t __arm_cx2a(int coproc, uint64_t acc, uint32_t n, uint32_t imm); |
| CX2DA | uint64_t __arm_cx2da(int coproc, uint64_t acc, uint32_t n, uint32_t imm); |
| CX3 | uint32_t __arm_cx3(int coproc, uint32_t n, uint32_t m, uint32_t imm); |
| CX3D | uint64_t __arm_cx3d(int coproc, uint32_t n, uint32_t m, uint32_t imm); |
| CX3DA | uint64_t __arm_cx3da(int coproc, uint64_t acc, uint32_t n, uint32_t m, uint32_t imm); |
| CX2 | uint32_t __arm_cx2(int coproc, uint32_t n, uint32_t imm); |

Table 3 Built-in functions supported by FCAU

| Instruction type | Built-in functions |
|---|---|
| VCX2 | uint32_t __arm_vcx2(int coproc, uint32_t n, uint32_t imm); |
| VCX3 | uint32_t __arm_vcx3(int coproc, uint32_t n, uint32_t m, uint32_t imm); |

Through these built-in functions, G32R5xx renames the instructions in Zidian. Table 4 uses VCX3 as an example and lists renamed VCX3 functions in Zidian.

Table 4 VCX3 renamed functions

| Instruction | Zidian function |
|---|---|
| VCX3 0, Sd, Sn, Sm, #0x0 | DIVF32 Sd, Sn, Sm |
| VCX3 0, Sd, Sn, Sm, #0x1 | QUADF32 Sd, Sn, Sm |
| VCX3 0, Sd, Sn, Sm, #0x2 | DIVF32_ATAN2 Sd, Sn |

# 3 Using Zidian to accelerate computation

## 3.1 zidian_math.h

In “zidian_cde.h”, built-in functions are renamed through macros. To use Zidian for regular mathematical operations in driverlib, include “zidian_math.h”. See the "Combining driverlib with Zidian" section for details.

“zidian_math.h” repackages commonly used mathematical functions. Table 5 lists the mathematical functions packaged in “zidian_math.h”.

Table 5 zidianmath functions

| Zidian function | Description |
|---|---|
| sinpuf32 | Calculate the sine value |
| sin | Normalize to the [0, 2π) interval, then calculate sine |
| cospuf32 | Calculate the cosine value |
| cos | Normalize to the [0, 2π) interval, then calculate cosine |
| atanpuf32 | Calculate the arctangent value |
| atan | Calculate the arctangent value |
| mpy2pif32 | Single-precision floating-point multiply |
| div2pif32 | Single-precision floating-point divide |
| sqrtf32 | Square root of a single-precision floating-point number |
| divf32 | Floating-point division |
| quadf32 | Calculate the quadrant values of X and Y |
| divf32_atan2 | Calculate the ratio of X to Y |
| atan2puf32 | atan2 |
| atan2 | atan2 |

## 3.2 Compiler support

The SDK currently provides MDK-ARM and IAR environments. Enabling Zidian support differs slightly by compiler.

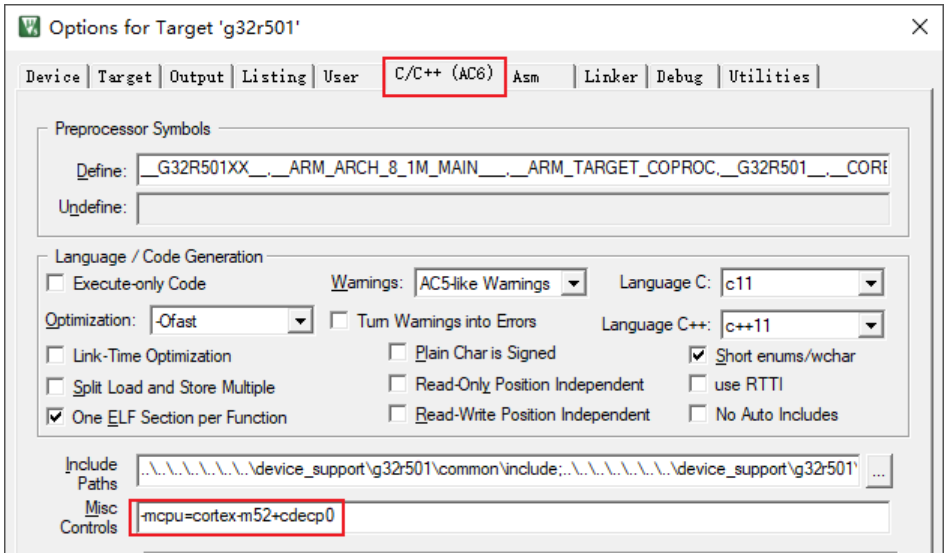
**Note:** The figures in this section use G32R501 as the example.

### 3.2.1 MDK-ARM (AC6)

Under C/C++ (AC6) → Misc Controls, add the following option for the device in use:

- G32R501: “-mcpu=cortex-m52+cdecp0”
- G32R502: “-mcpu=cortex-m52+nomve.fp+nofp.dp+cdecp0”

Figure 1 Enabling CDE in AC6



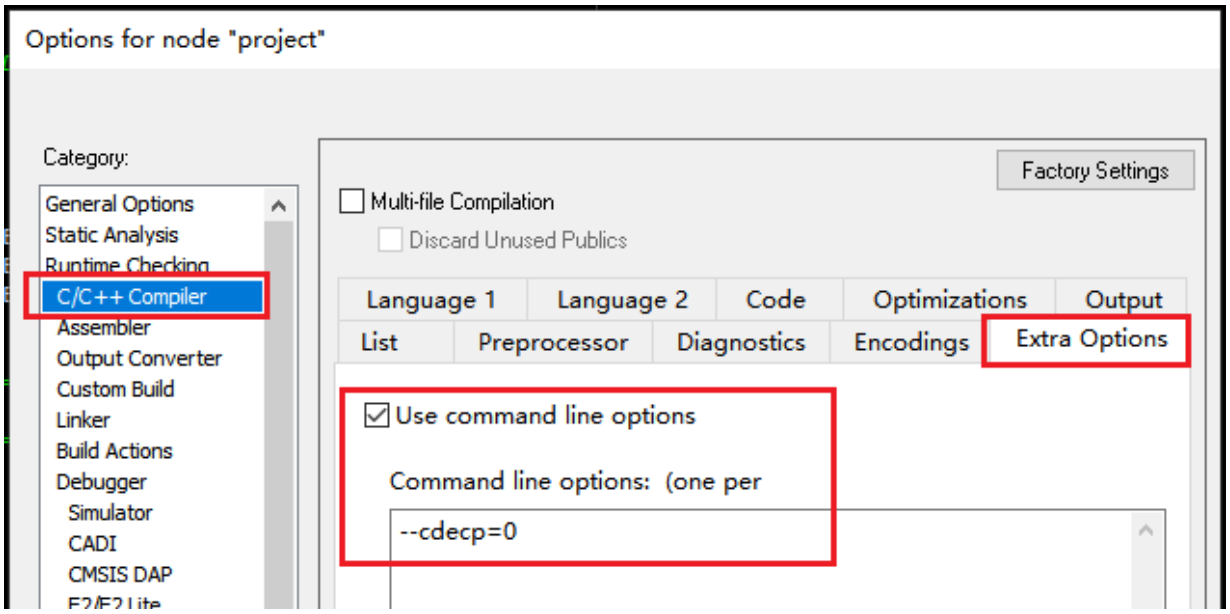

### 3.2.2 IAR (ICC)

IAR Embedded Workbench for Arm support is compilation support.

Enable it under C/C++ Compiler → Extra Options: select Use command line options, then add:

- G32R501 and G32R502: “--cdecp=0”

Figure 2 Enabling CDE compilation in ICC




## 3.3 Software design examples

This section uses the MDK-ARM environment as an example of accelerating computation with Zidian.

### 3.3.1 Combining driverlib with Zidian

Steps for using Zidian in an SDK driverlib example:

1. Enable compiler support.
2. Add the “ZIDIAN_FCAU” macro under the project C/C++ options to redirect trigonometric functions supported by Zidian.
3. Include “zidian_math.h” in source files that need Zidian.

This note follows the SDK driverlib example “zidian_ex1_math”.

The example uses Zidian to exercise “sqrt”, “sin”, “cos”, “atan”, and “atan2”. Because these functions are already packaged in “zidian_math.h”, include that header and call them directly:

```
# include "zidian_math.h"

// Main
void example_main(void)
{
    volatile float x, y;
    uint16_t i;
    // Test1 sqrtf
```

```
    x = 0.81f;
    GET_DWT_CYCLE_COUNT(dwtCycleCounts[0], trace1Result[0] = sqrtf(x));
    for (i = 0; i < COUNT; i++)
    {
        trace1Result[i] = sqrtf(x);
    }
    // Test2 sinf
    x = PI / 2;
    GET_DWT_CYCLE_COUNT(dwtCycleCounts[1], trace2Result[1] = sinf(x));
    for (i = 0; i < COUNT; i++)
    {
        trace2Result[i] = sinf(x);
    }
    // Test3 cosf
    x = PI / 4;
    GET_DWT_CYCLE_COUNT(dwtCycleCounts[2], trace3Result[2] = cosf(x));
    for (i = 0; i < COUNT; i++)
    {
        trace3Result[i] = cosf(x);
    }
    // Test4 atanf
    x = 5.0f;
    GET_DWT_CYCLE_COUNT(dwtCycleCounts[3], trace4Result[3] = atanf(x));
    for (i = 0; i < COUNT; i++)
    {
        trace4Result[i] = atanf(x);
    }
    // Test5 atan2f
    x = 5.0f;
    y = 10.0f;
    GET_DWT_CYCLE_COUNT(dwtCycleCounts[4], trace5Result[4] = atan2f(y, x));
    for (i = 0; i < COUNT; i++)
    {
        trace5Result[i] = atan2f(y, x);
    }
    // Loop
    for (;;)
    {
    }
}
```

### 3.3.2 Combining the math library with Zidian

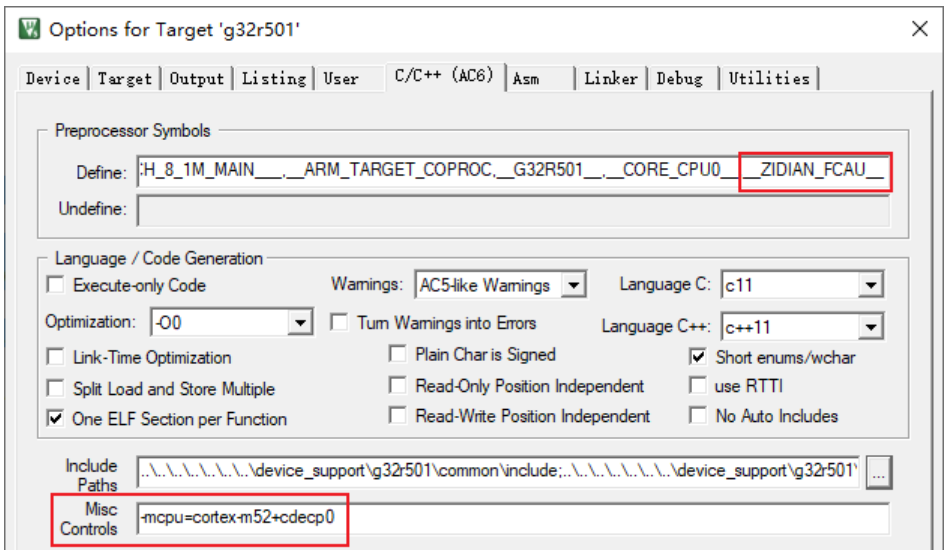
To accelerate math-library calls with Zidian:

1. Enable compiler support.
2. Add the “ZIDIAN_FCAU” macro under the project C/C++ options to redirect math-library functions supported by Zidian.

Take an FPUfastRTS example as reference. Because “sin”, “cos”, and related functions are packaged in FPUfastRTS, calling them without “ZIDIAN_FCAU” uses the FPUfastRTS implementations.

To use Zidian acceleration, add the macro in the corresponding project C/C++ options, then call the target functions.

Figure 3 Using Zidian acceleration in the math library




After enabling compiler support and adding “ZIDIAN_FCAU”, call the functions directly:

```
in.f32 = test_input[i];
// Run the calculation function and measure the DWT cycle count simultaneously
GET_DWT_CYCLE_COUNT(dwtCycleCounts[0], out.f32 = atanf(in.f32));
test_output[i] = out.f32;
```

# 4 Revision

Table 6 Document revision

| Date | Version | Description |
|---|---|---|
| 2025.1 | 1.0 | ● Initial release |
| 2026.8 | 1.1 | ● Listed applicable products as G32R501 and G32R502<br>● Refined the comparison table by function family from “zidian_cde.h” / “zidian_math.h”<br>● Clarified 501-only FFT/complex/CX3·CX3D, 502-only div 64 and CRC wrappers, and shared FCAU plus CRC macros. |

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